Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OC**
2. **1Q**
3. **ID**
4. **2D**
5. **2Q**
6. **3Q**
7. **3D**
8. **4D**
9. **4Q**
10. **GND**
11. **LE**
12. **5Q**
13. **5D**
14. **6D**
15. **6Q**
16. **7Q**
17. **7D**
18. **8D**
19. **8Q**
20. **VCC**

**.082”**

**3 2 1 20 19 18**

**17**

**16**

**15**

**14**

**8 9 10 11 12 13**

**4**

**5**

**6**

**7**

**.082”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: B**

**APPROVED BY: DK DIE SIZE .082” X .082” DATE: 10/13/21**

**MFG: NATIONAL THICKNESS .014” P/N: 54HCT373**

**DG 10.1.2**

#### Rev B, 7/1